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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant Seon Ho HAN et al	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT NUMBER	ISSUE DATE	PATENTEE	CLAS S	SUB- CLAS S	FILING DATE IF APPROPRIATE
	5 1 7 9 3 5 9	01/12/93	McLeod	-	-	
	5 7 3 9 7 3 0	04/14/98	Rotzoll	-	-	
	6 0 2 8 4 8 8	02/22/00	Landman et al	-	-	
	6 1 3 7 3 7 2	10/24/00	Welland	-	-	
	6 5 9 7 2 4 9	07/22/03	Chien et al	-	-	

FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

EXAMINER INITIAL	DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUB- CLASS	TRANSLATION YES NO
	2002 0 0 6 9 6 8 5	09/05/02	Korea			

OTHER DOCUMENTS (Including Author, Title, Date, Place of publication)

	Chi-Wa Lo et al, "A 1.5-V 900-MHz Monolithic CMOS Fast-Switching Frequency Synthesizer for Wireless Applications," 2000 Symposium on VLSI Circuits Digest of Technical Papers, pp. 238-241
	Frank Herzel et al, "An Integrated CMOS PLL for Low-Jitter Applications," IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing, Vol. 49, No. 6, June 2002, pp. 427-429
	Tsung-Hsien Lin et al, "A 900MHz, 2.5mA CMOS Frequency Synthesizer with an Automatic SC Tuning Loop," Electrical Engineering Department, University of California, Los Angeles CA 90095-1594, pp. 375-378
	Yido Koo et al, "A Fully-Integrated CMOS Frequency Synthesizer with Charge-Averaging Charge Pump and Dual-Path Loop Filter for PCS- and Cellular-CDMA Wireless Systems," 2001 Symposium on VLSI Circuits Digest of Technical Papers, pp. 43-46
EXAMINER	DATE CONSIDERED 1/30/08
EXAMINER: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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